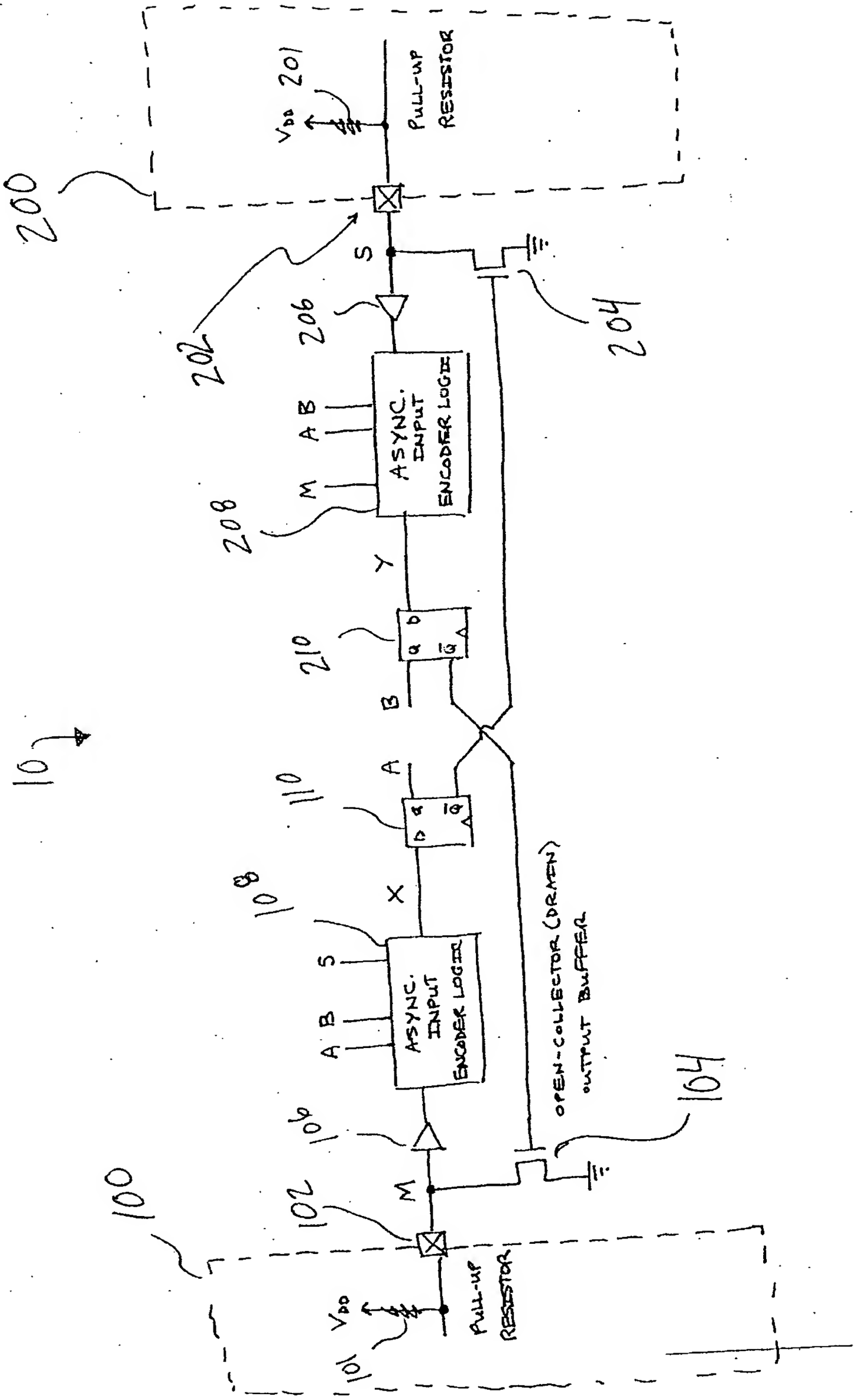
10
100
101
102
104
106
108
110
200
201
202
204
206
208
210
V_{DD}
PULL-UP RESISTOR
S
M
X
Y
A
B
ASYNC. INPUT ENCODER LOGIC
OPEN-COLLECTOR (DRAIN) OUTPUT BUFFER

FIG. 1

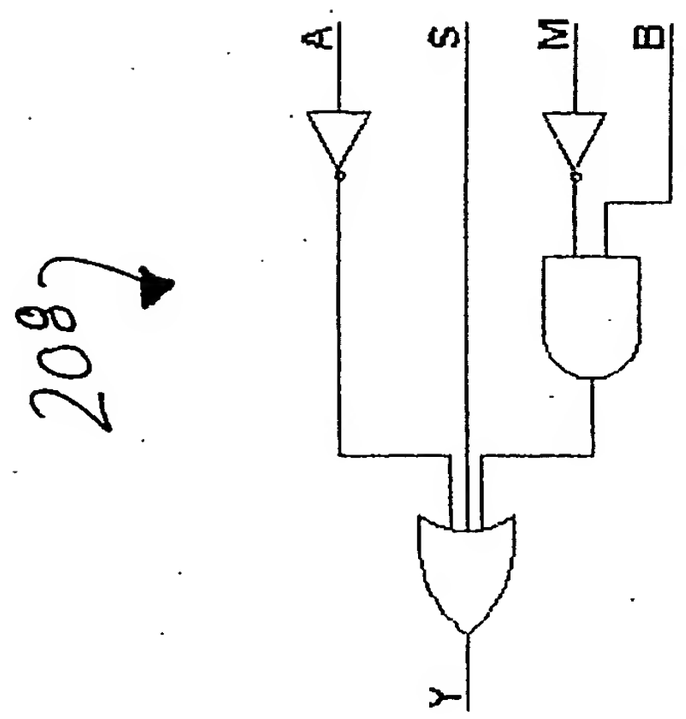

FIG. 2B

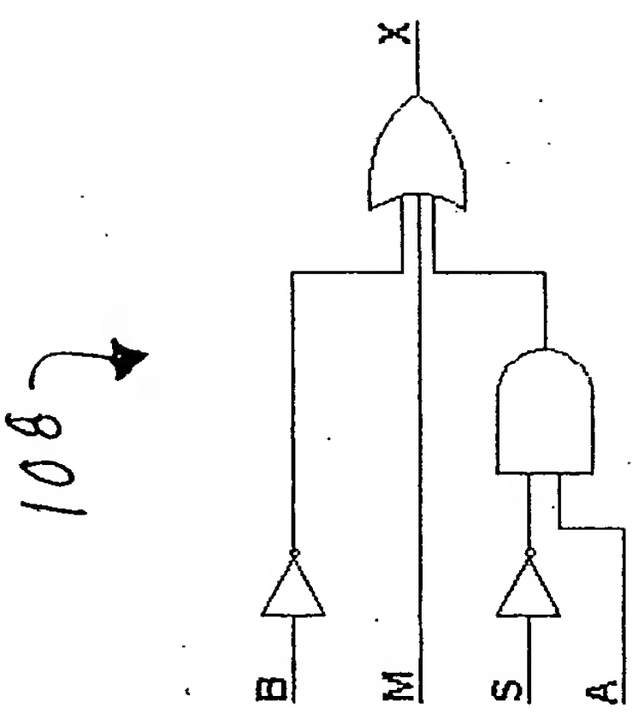

FIG. 2A

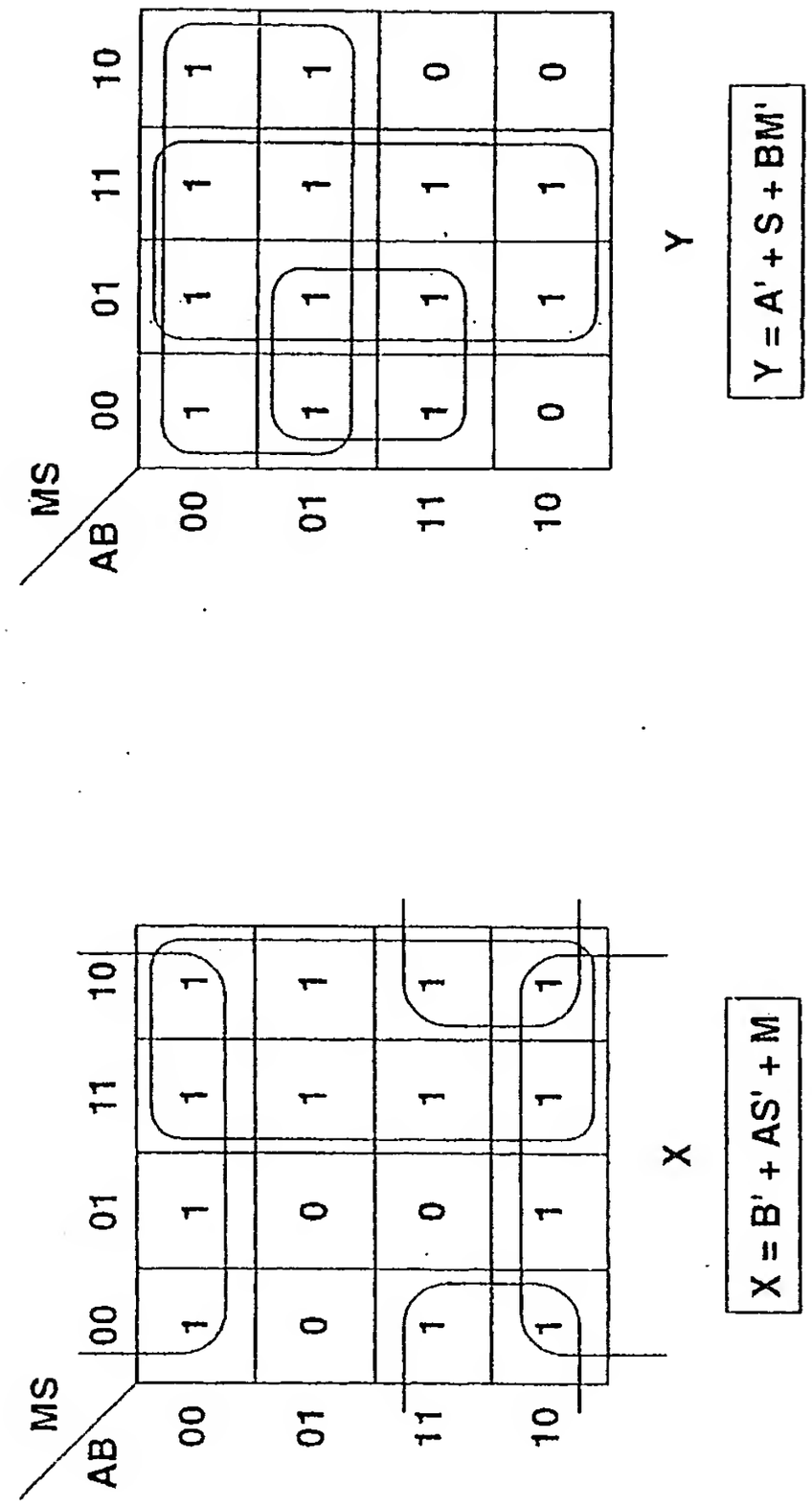

FIG. 3

Present State		Inputs	Next State	
A	B	M	S	X	Y
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	1	1	1
0	0	1	0	1	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	1	1	1
0	1	1	0	1	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1
1	1	1	0	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	1	1	1
1	0	1	0	1	0

FIG. 4

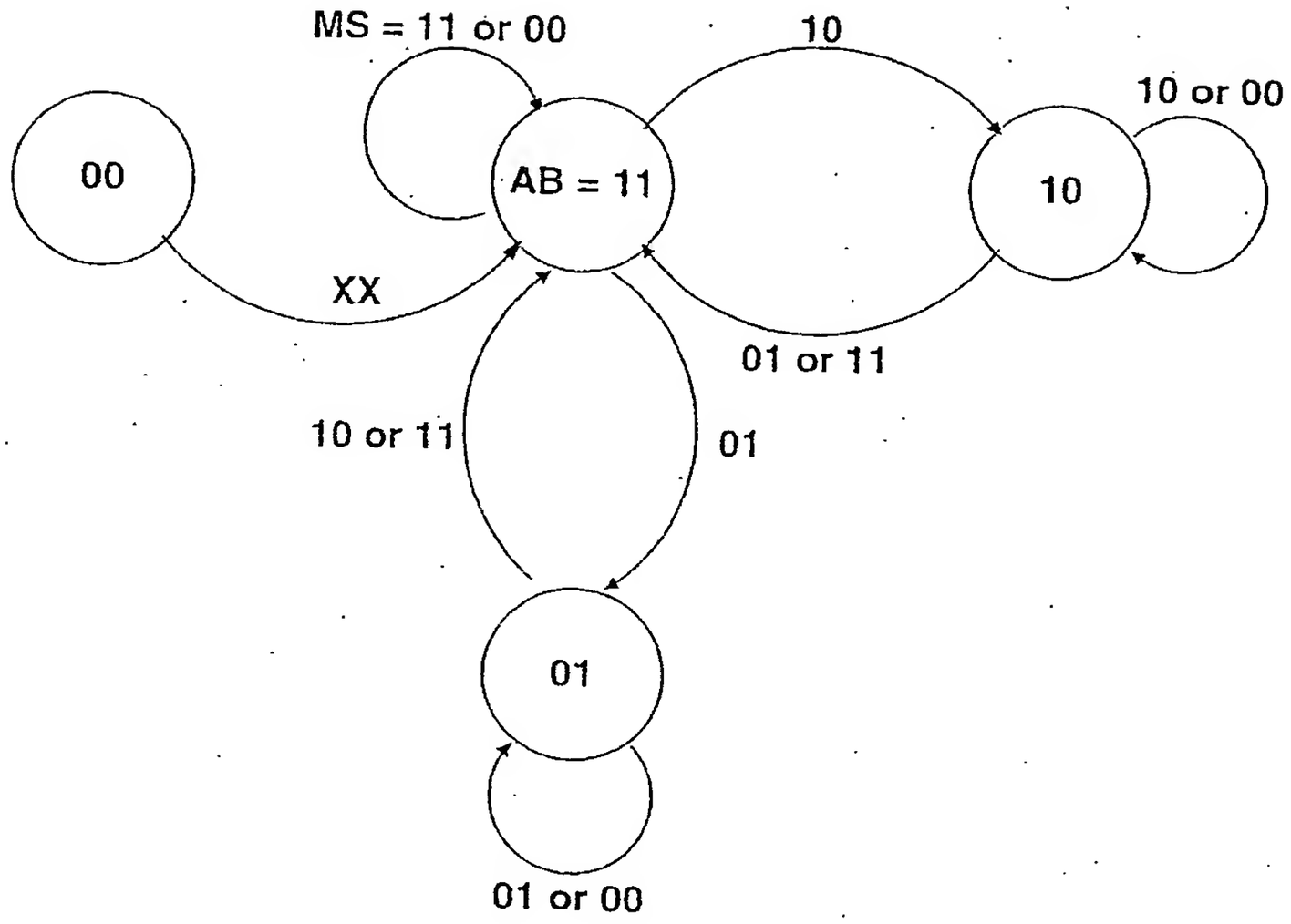

FIG. 5

Time	Event	Result	Transition Tested
0s	Start	Clock running. Inputs Undefined.	
52ns	Master drives HIGH	Slave follows HIGH on next clock pulse; State Transitions to AB = '11'	h
102ns	Master drives LOW	Slave follows LOW on next clock pulse; State Transitions to AB = '01'	e
152ns	Master drives HIGH	Slave follows HIGH on next clock pulse; State Transitions to AB = '11'	f
176ns	Master releases.	State remains at AB = '11'	
202ns	Slave drives LOW	Master follows LOW on next clock pulse; State Transitions to AB = '10'	b
252ns	Slave drives HIGH	Master follows HIGH on next clock pulse; State Transitions to AB = '11'	d
302ns	Master AND Slave drive LOW	State remains at AB = '11'	a
352ns	Master AND Slave drive HIGH	State remains at AB = '11'	a
375ns	Slave releases.	State remains at AB = '11'	
402ns	Master drives LOW	Slave follows LOW on next clock pulse; State Transitions to AB = '01'	e
452ns	Slave drives HIGH	State remains at AB = '01'	g
476ns	Slave releases.	Slave follows LOW on next clock pulse; State remains AB = '01'	g
552ns	Master AND Slave drive HIGH	State Transitions to AB = '11'	f
625ns	Master releases.	State remains at AB = '11'	
652ns	Slave drives LOW	Master follows LOW on next clock pulse; State Transitions to AB = '10'	b
702ns	Master drives HIGH	State remains at AB = '10'	c
725ns	Master releases.	Master follows LOW on next clock pulse; State Remains AB = '10'	c
802ns	Master AND Slave drive HIGH	State Transitions to AB = '11'	d

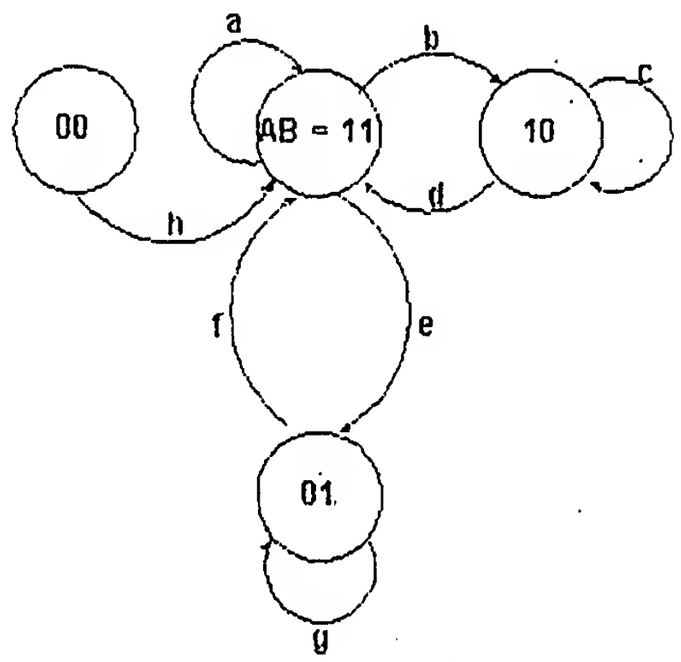

FIG. 6

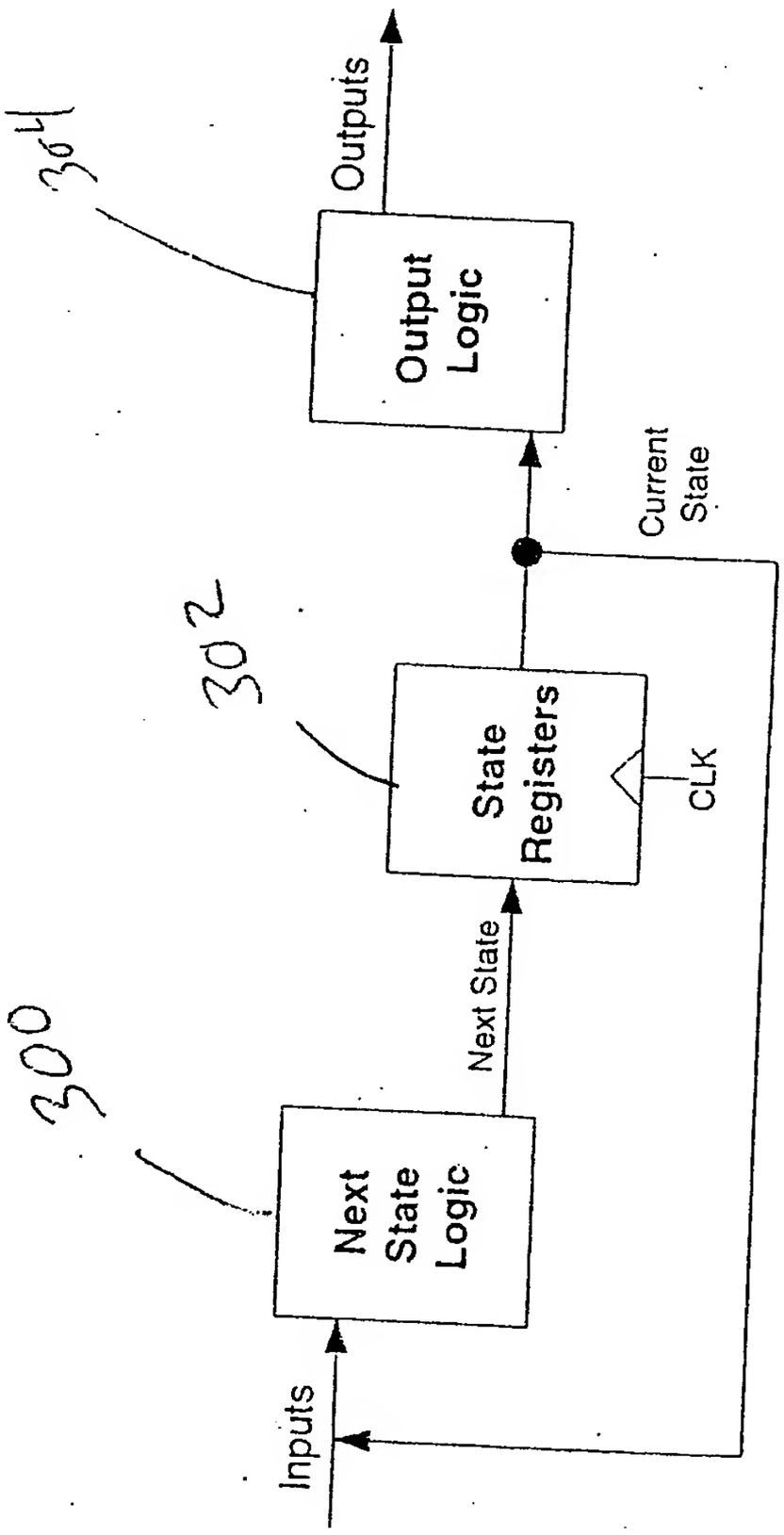
304
Outputs
Output Logic
Current State
302
State Registers
CLK
Next State
300
Next State Logic
Inputs

FIG. 7